Statistical Post-Processing at Wafersort – An Alternative to Burn-in and a Manufacturable Solution to Test Limit Setting for Sub-micron Technologies.

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Abstract

In sub-micron CMOS processes, it has become increasingly difficult to identify and separate outliers from the intrinsic distribution at test. This is due to the increasing inadequacy of reliability screens such as burn-in and IDDQ testing. Statistical Post-Processing (SPP) methods have been developed to run off-tester using the raw data generated from Automatic Test Equipment (ATE) and wafersort maps. Post-Processing modules include advanced IDDQ tests such as Delta IDDQ and the Nearest Neighbor Residual (NNR), as well as other non-IDDQ based reliability-focused modules. This work presents the application and results of SPP at LSI Logic on 0.18um CMOS products. Challenges of production implementation have been overcome, which include "user definable" adaptive threshold limits, handling multiple data sources, and data flow management. Burn-in data and customer Defects per Million units (DPM) data show a 30-60% decrease in failure rate with SPP implementation with very acceptable yield loss.

1.0 Introduction

The measure of quiescent current provides extended fault coverage due to the inherently wide observability of the power supply rails for static CMOS designs. However, the static leakage growth for deep sub-micron technologies has obscured the defect resolution of IDDQ testing. In order to use IDDQ effectively, methods of variance reduction in the IDDQ data sets are required. Two complementary methods of advanced IDDQ testing for deep sub-micron technologies include Delta Iddq and NNR.

Delta IDDQ and similar intra-die based vector methods have been described in the literature, some examples can be found in [1,3,5,6]. A calculated delta is compared to a threshold that is less difficult to set than that needed for traditional IDDQ testing due to the reduction in variance of the delta distributions [2]. Small IDDQ test sets, however, may cause a defect to escape Delta IDDQ detection. There must be at least one vector activating and one vector not activating a defect to identify the defect with Delta IDDQ. Using an inter-die approach, such as NNR, in a complementary fashion allows those defective die with all vectors activating the defect to be screened. NNR is an effective variance reduction technique that uses the parametric data from neighboring die locations for predicting test outcomes of a die [2, 7]. For this implementation, NNR is used on IDDQ data. An important concept in this work is the complementary method in which Delta Iddq and NNR are used as an improvement to IDDQ testing.

It is possible that a test set may not activate the defect at all. In this case no defect IDDQ signature is available in the IDDQ data. For this reason, additional modules have been included in the SPP methodology at LSI.

Other non-Iddq based test methods such as minVDD or Very Low Voltage (VLV) testing have also been shown to be important methods to screen resistive path and delay defects [8]. Also the behavior of defects under temperature has been shown to be different to that of defect free die [8]. The major challenge for these test methods is to understand how to identify and screen the defective die in production without excessive yield loss of defect free die.

Targeting defect regions as a specific screening method can be an important tool for increasing reliability. Researchers have looked at the yield of the region surrounding a particular die to make predictions about the reliability of that die [4, 9]. Binning even the seemingly healthy die in or near wafer regions of low

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yield as fails eliminates high probability reliability fails from the final distribution.

2.0 Production motivation at LSI Logic

A new approach for test pass/fail decision-making in production at LSI was required for various reasons. These included:

a) Single IDD threshold or stepped IDD threshold limits derived from die speed was leading to high yield loss due to increasing transistor leakage in specific areas such as the edge of wafer (Figure 1) and resulting in high burn-in Early Fail Rate (EFR) and customer fails (DPM) due to ineffectiveness of screening die outside the typical distribution (Figure 2, 3 and 4))

b) At the introduction of new process technologies higher defect densities (i.e. low yields) caused higher Early Failure Rates (EFR) and DPM levels (Figure 4). High yield loss occurred from the more stringent test screening that had to be applied to maintain consistent DPM levels.

c) Fluctuations in fabrication defect density cause lots with higher risk to be shipped to the customer. Rather than scrapping these lots at high cost, post processing techniques were needed to identify statistical outliers and at-risk die in bad neighborhoods and reject or send these die for burn-in.

d) High burn-in costs and the decreasing effectiveness of burn-in due to thermal runaway and voltage acceleration limitations [8] have placed more importance on outlier screening by alternative means

e) On-tester outlier screening is difficult due to the need to vary the limits depending on the die location and the intrinsic distribution of the good die across the wafer and lot being tested. A single outlier screening technique is not adequate or effective.

f) Resistive path and delay fault defects caused by partial opens are becoming increasingly difficult to pick-up at test. These defect mechanisms are also generally harder to screen with voltage stressing (burn-in or stress testing). Minimum VDD testing has been shown to identify the outliers from the intrinsic distribution, but applying a threshold limit on tester is very difficult without experiencing a high invalid yield loss (See Figure 3).

The following figures illustrate the problems identified in the list above. For example, Figure 1 illustrates the commonly seen inadequacy of using a single threshold limit. This is a composite map of failing die locations due to the application of a single threshold. High yield loss occurs on the edge because those devices are faster and therefore have a higher level of intrinsic leakage, and not because they are defective.

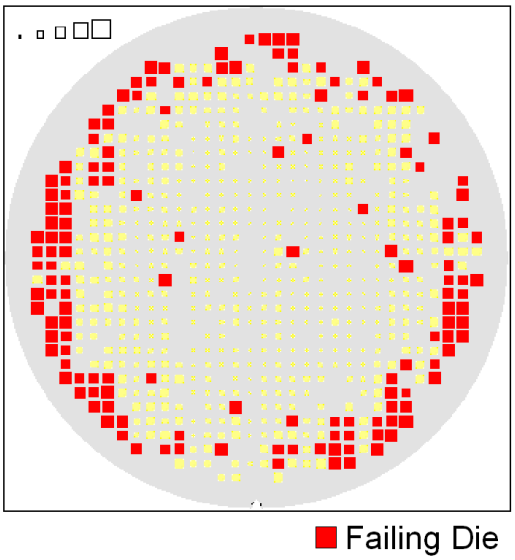

Figure 1. A Composite wafer map for a single product. The size of each square is proportional to the number of failing die at a particular site. Excessive yield loss is observed at wafer edge due to single threshold IDDQ limits.

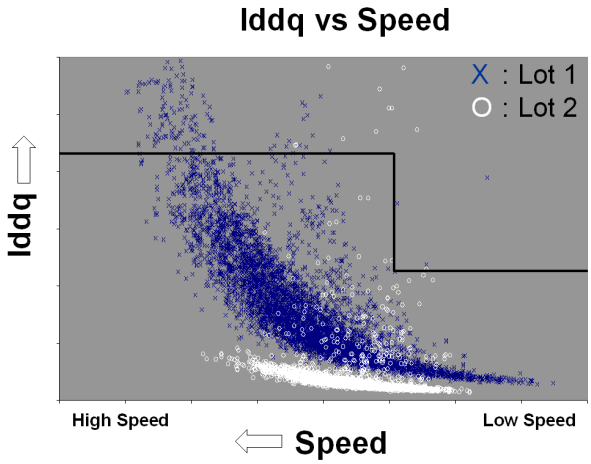

Figure 2. IDDQ vs. speed plot for LSI 0.18 um process. Stepped threshold limits lead to unnecessary yield loss at faster end on LOT 1 but do not adequately screen outliers on the slower end especially on LOT 2. Both lots are the same product and were fabricated and tested at the same location.

As an improvement to the single threshold problem, Figure 2 illustrates a method of stepping the IDDQ threshold by utilizing speed measurements of the die. The measured speed places the die into a category that uses a specific IDDQ threshold. However, as seen in Figure 2, this method can also lead to poor coverage and excessive yield loss. The IDDQ versus speed for two lots of the same product from the same fab are displayed. While both lots have poor outlier coverage with the stepped threshold, lot1 also has excessive yield loss on the high-speed end. Similarly, Min VDD testing can help to identify outliers as shown in Figure 3. Clearly the outliers are visible, but setting the limit on the tester without causing high yield loss becomes difficult.

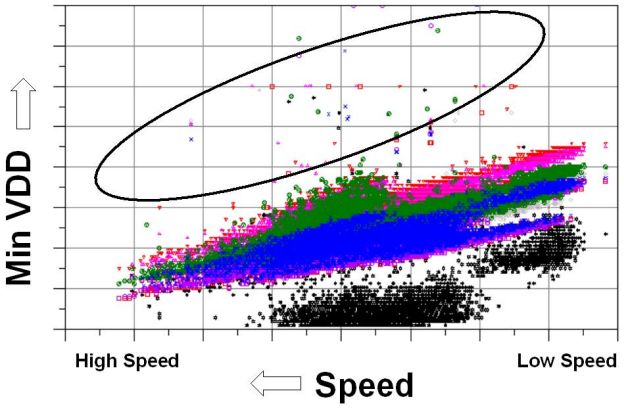

Figure 3. Minimum VDD results for different functional tests clearly showing min VDD outliers (circled).

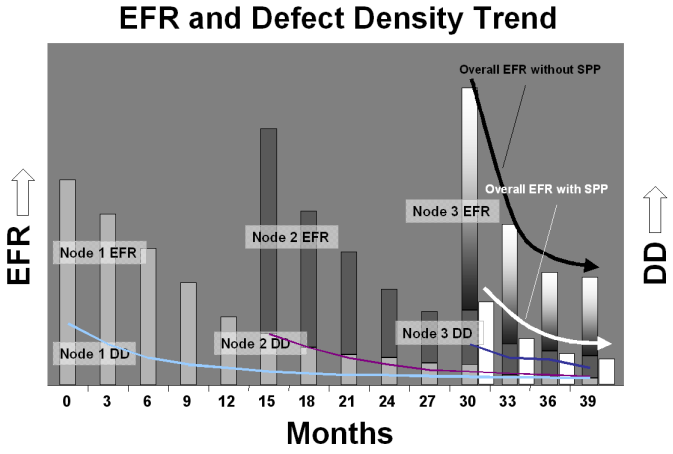

Figure 4. EFR and Defect density trend. Higher initial defect densities and spikes in EFR levels are observed with the introduction of smaller technology nodes. SPP with "user definable" stringency can dampen that effect as seen in the EFR data for the Node 3 lots that were processed through SPP.

The result is that statistical outliers are sent to the customer. One example of parametric data gathered from customer returns has identified approximately 40% of these returns as belonging to the IDDQ versus Speed outlier region. The SPP methodology implemented at LSI Logic will significantly reduce the number of outlier die that are sent to the customer. Figure 4 gives an indication of the reduced EFR rate that can be achieved through SPP application with respect to various levels of defect density for advanced technologies.

3.0 Statistical Post-Processing Modules

The following modules have been or are being developed at LSI to run off-tester. These modules can be applied to IDDQ and non-IDDQ test methods and also to tests at different temperatures.

3.1 Intra-die vector based modules

Intra-die modules have been developed to identify defective die on which the defects effect some but not all of the vector values. The effectiveness of such modules depends on the availability of vectors like IDDQ for which multiple readings are taken per die to achieve proper test coverage. Intra-die vector based algorithms compute the differences between vector values on the same die, compare the differences against an expected difference to get a residual which is then measured against a threshold to determine a downgrade. The threshold value itself is adaptive (i.e. data-driven) and will vary from die to die as explained in Section 5.0.

3.2 Inter-die vector based modules

Defective die in which the defect effects all the vector values, or die with passive defects that do not result in differences greater than the threshold value will not be picked up by the modules discussed above. Modules and algorithms that compare a vector average for each die against the expected value for that site pick up such dies. The expectation, based on the vector averages of the surrounding sites, is used to compute a residual, which is compared to an adaptive threshold value to flag outlier die.

3.3 Inter-die non-vector based modules

A set of reliability-focused modules has been deployed to provide "user definable" downgrade capability. Neighbor Association Exclusion (NAE) is one such module that downgrades "good" die in "bad" neighborhoods, assuming that they are actually at-risk die. The NAE threshold, which defines acceptable yield in the die neighborhood, is user definable and can be adjusted to accommodate the confidence in the maturity of a technology and acceptable EFR values (Figure 5).

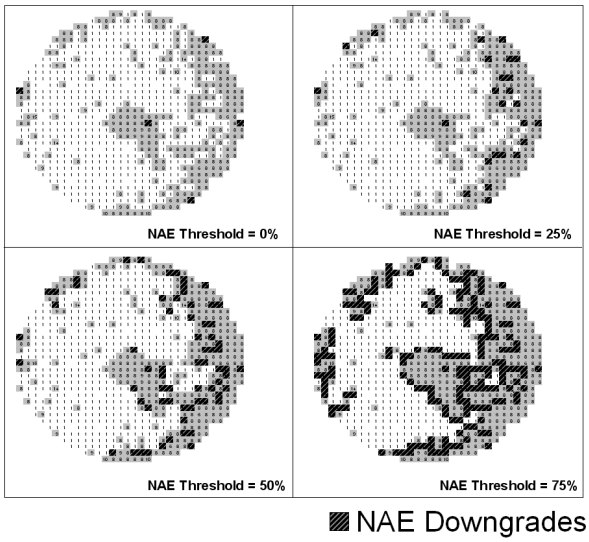

Figure 5. The NAE algorithms downgrade "good" die in "bad" neighborhoods. The number of downgrades depends on a user definable threshold.

3.4 Site or location based modules

Site and location based SPP modules are mainly reliability enhancing modules. These include algorithms to downgrade good die in sites that are determined to be at-risk due to either process or reticle issues. These modules are generally applied on an as-needed basis to avoid full wafer scraps and ensure reliability of the shipped die.

3.5 Future modules under development

Statistical Post-Processing of data from combinations of tests is another method of differentiating between defective and defect free die. An example of this would be comparing test results at different voltages or temperatures and identifying die with significantly different behavior from the intrinsic distribution. Using die tracing techniques, it is possible to compare results at final testing to the results for the same die at wafersort and process the data for outliers based on both test results. This may be an important technique for very deep sub-micron defect screening.

4.0 Variable Thresholds

The models for each both identify a residual defined as the difference between estimates of the defect free IDDQ current for a die and its actual IDDQ current. Threshold setting adopted for the residual includes an effective overlapping of minimum and variable limits, compensating for the large range of intrinsic IDDQ. The defect component of the residual dominates the estimation error component flagging the die as an outlier. In the application of these modules, the level of intrinsic current for a die is eliminated as a factor for the IDDQ test. This factor is the cause for the downfall of the traditional IDDQ test. Thus, defect resolution is obtained for die across the intrinsic leakage spectrum for a wafer.

The vector modules discussed earlier reduce the intra-die or inter-die vector differences to a residual by comparing the vector value against an expected value. Ideally this residual value will be equal to zero for good die and non-zero for outliers. Estimate noise introduced due to factors like tester resolution and natural variation across data sets results in a residual distribution around zero. Furthermore the estimate noise varies as a function of the intrinsic estimate of the vector due to technology boundary conditions such as process control on the wafer edge, shrinking gate oxide thickness and shorter channel lengths.

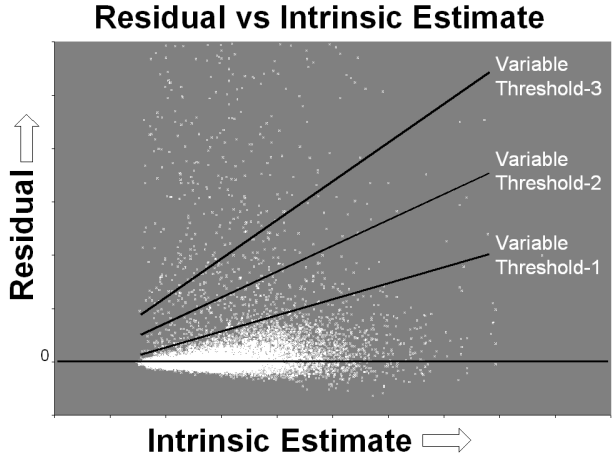

Figure 6. A simple relation defines the boundary between good die and outliers when residuals are plotted against the intrinsic estimate. Variable thresholds can be set to define this boundary for desired EFR values and/or SPP fallout.

A plot of the residual as a function of the intrinsic estimate of the vector indicates that a simple relation can be established for each process technology to differentiate between the good die and the outliers or at-risk die (Figure 6). This relation can then be used to generate adaptive variable thresholds and can also be adjusted to achieve the desired EFR and acceptable fallout due to downgrades (Figure 7).

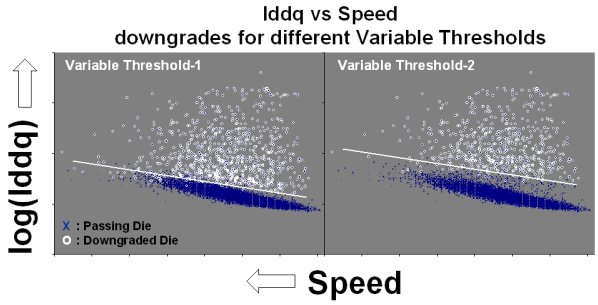

Figure 7. Different variable threshold settings can be used to achieve the required EFR and acceptable SPP yield loss.

The adaptive nature of the threshold, i.e. the fact that the threshold is defined by a function rather than a static value, ensures that the same settings will result in comparable SPP downgrade efficiency irrespective of the actual distribution of the data. In other words the outliers will be downgraded with equal certainty on both lot 1 and lot 2 in Figure 2 using the same SPP settings.

5.0 Production Implementation

The prerequisites for a test floor to be able to run Statistical Post Processing in production are as follows:

a) Automated bin data collection;
b) Full ATE parametric data collection;
c) Inkless wafer map generation for assembly;

The basic flow of the above listed data types in described in Figure 8. Bin and ATE Parametric data are fed into converters to provide the SPP modules with raw data in a predefined format. The SPP modules apply product specific setups, which control the specific modules and the thresholds to be applied, and generate a revised Bin assignment which is then used to generate the inkless map for assembly and is converted back to the site specific format for further propagation to analysis and disposition systems. This allows the SPP code, setups and algorithms to be centrally managed and at the same time provides a clear interface to implement the program at any site irrespective of the local data formats.

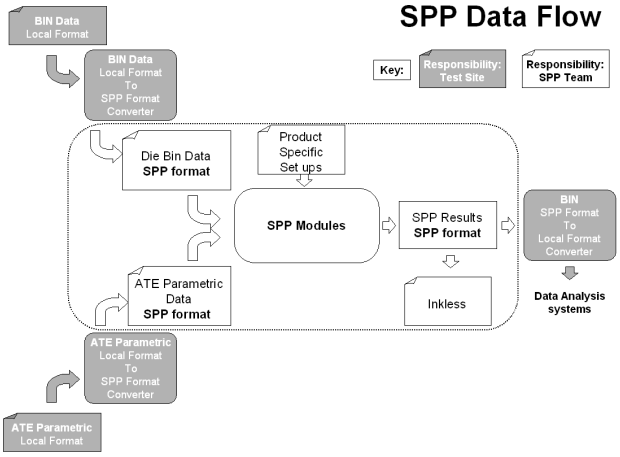

Figure 8. Data flow for SPP implementation.

The current implementation allows centralized program control while having no run-time impact on tester utilization or uptime. Under normal operating conditions when the network is available, the tester calls the SPP program with a trigger and sends the Pre-SPP test results over the network. SPP is applied and the Post-SPP results are returned to the tester. The whole operation is completed in well under 25% of the time it takes for the tester to load and start testing on the next wafer, thus having no impact on tester cycle time.

A provision has been made on both the tester and server to queue the data and triggers incase the network is not available. This ensures that when the network is down the tester can still continue testing wafers. When the network becomes available the queue is processed and operations return to normal in a matter of minutes.

6.0 Burn-in and Yield results

As indicated earlier, from a sample of returns, approximately 40% of the returns were statistical outliers. By SPP implementation, these units will be screened and therefore a commensurate 40% decrease in customer DPM (fault coverage related) can be expected. Figure 9 illustrates that the yield fallout due to SPP fails as the defect density decreases. The variation from lot to lot for similar defect densities can be explained by varying degrees of clustering which has an impact on all the SPP modules.

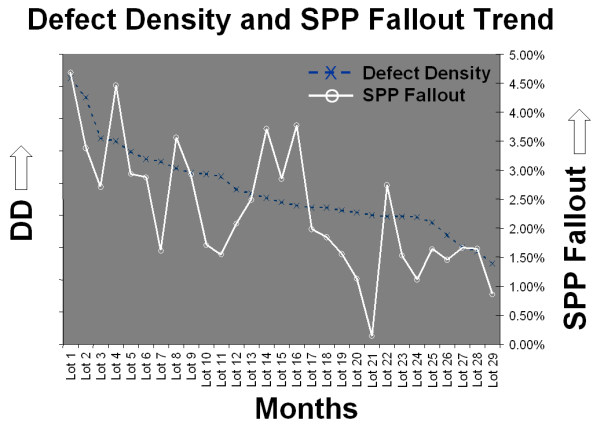

Figure 9. Yield Fallout due to SPP decreases as defect density decreases.

To gauge the impact on EFR improvement 14 lots with a total of 60,105 passing die were sorted and processed through SPP. All the SPP downgrades and a sample of 1,388 die from the passing die were subjected to a 24-hour burn-in. The results shown in Table 1 indicate that of the 171 burn-in failures SPP downgrades picked up 168 of them resulting in a 50.2% reduction of overall EFR.

Lot ID	Total Passing Die	SPP Downgrades					Remaining Passing Die			
		% of Passing Die	Quantity	Burn-in			Quantity	Burn-in		
				Sample	# Fails	%Fail		Sample	# Fails	%Fail
Lot 1	3566	4.60%	163	163	25	15.34%	3403	0	0	0.00%
Lot 2	5320	3.74%	199	199	20	10.05%	5121	0	0	0.00%
Lot 3	5198	3.33%	142	142	15	10.56%	5056	0	0	0.00%
Lot 4	4620	2.79%	128	128	19	14.84%	4492	0	0	0.00%
Lot 5	5458	2.71%	144	144	0	0.00%	5314	444	0	0.00%
Lot 6	5458	2.64%	142	142	37	26.06%	5316	0	0	0.00%
Lot 7	5249	2.63%	137	137	16	11.68%	5112	0	0	0.00%
Lot 8	4580	2.62%	119	119	15	12.61%	4461	100	0	0.00%
Lot 9	4854	2.55%	121	121	6	4.96%	4733	0	0	0.00%
Lot 10	4888	2.39%	114	114	4	3.51%	4774	444	3	0.68%
Lot 11	5364	2.18%	106	106	4	3.77%	5258	100	0	0.00%
Lot 12	641	1.58%	10	10	0	0.00%	631	100	0	0.00%
Lot 13	4441	0.97%	41	41	7	17.07%	4400	100	0	0.00%
Lot 14	468	0.65%	3	3	0	0.00%	465	100	0	0.00%
Total	60105	2.68%	1,569	1,569	168	10.71%	58,536	1,388	3	0.22%

Table 1. Results of 24 hour burn-in experiment

7.0 Conclusion

A production worthy solution to outlier detection and re-binning using Statistical Post Processing (SPP) at wafersort is shown in this paper. Clear cost/benefit analysis has been presented in terms of early fail rate (50% improvement), customer DPM (40% improvement) and yield loss (0.6% - 2.5% depending on technology and gate count). Intra-die and inter-die vector and non-vector based SPP modules are described that work together to effectively and efficiently identify outlier die for IDDQ and non-IDDQ test methods. The concept of variable thresholds is introduced and explained to allow for tightening or loosening of fail criteria as technology matures or for process excursion and maverick lot control. Requirements for production implementation are documented. Data format and data flow challenges are overcome with bin data and ATE raw data collection and conversion to standard SPP formats. Future Post-processing modules are being developed for screening of VDSM resistive path defects and to extend the life of IDDQ effectiveness.

References

1. A. Gattiker, W. Maly, "Current Signatures," Proceedings VLSI Test Symposium, pp. 112-117, April 1996.

2. W.R. Daasch, J. McNames, D. Bockelman, K. Cota, R. Madge, "Variance Reduction using Wafer Patterns in IDDQ Data," Proceedings ITC, pp. 189-198, October 2000.

3. C. Thibeault, "Improving Delta-IDDQ-based Test Methods," Proceedings ITC, pp. 207-216, October 2000.

4. W.C. Riordan, R. Miller, J. M. Sherman, J. Hicks, "Microprocessor Reliability Performance as a Function of Die Location for a 0.25u, Five Layer Metal CMOS Logic Process," International Reliability Physics Symposium, pp. 1-11, March 1999.

5. T.J. Powell, J. Pair, M. St.John, and D. Counce, "Delta IDDQ for Testing Reliability", 18th IEEE VLSI Test Symposium, 2000, pp439-443.

6. S. Jandhyala, H. Balachandran, M. Sengupta, and A.P. Jayasumana, "Clustering Based Evaluation of IDDQ Measurements: Applications in Testing and Classification of Ics", 8th IEEE VLSI Test Symposium, 2000, pp444-448.

7. R. Daasch, K. Cota, J. McNames, R. Madge, "Neighbor Selection for Variance Reduction in IDDQ and Other Parametric Data", ITC, 2001.

8. P. Nigh, A. Gattiker, "Test Method Evaluation Experiments and Data", ITC, 2000, pp199-206.

9. T.S. Barnett, A. D. Singh, V.P. Nelson, "Burn-in fails and local region yield and integrated yield/reliability model", Proceedings VLSI Test Symposium, pp. 326 – 332, April 2001.